Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (Original): An imager system provided in a semiconductor substrate comprising:

a plurality of photosensitive, charge integrating pixels arranged in rows and columns of a pixel array for capturing illumination of a scene to be imaged, each pixel comprising a photogenerated charge accumulation region of the substrate and a sense node at which an electrical signal, indicative of pixel charge accumulation, can be measured without discharging the accumulation region;

pixel access control circuitry connected to pixel array rows and columns to deliver pixel access signals generated by the access control circuitry for independently accessing a selected pixel in the array;

an input interface circuit connected to accept a dynamic range specification input for the array pixels;

integration control circuitry connected to access a selected pixel of the array to read the sense node electrical signal of the selected pixel, and configured to generate pixel-specific integration control signals delivered to the selected pixel, independent of other pixels, based on dynamic range specification input provided by the input interface circuit; and

an output interface circuit connected to the pixel array to produce output image data based on sense node electrical signals from the pixel array.

2. (Original): The imager system of claim 1 wherein the pixel sense node electrical signal comprises a voltage signal.

3. (Original): The imager system of claim 1 wherein the charge integrating pixels comprise CMOS pixels.

4. (Original): The imager system of claim 1 wherein the pixel-specific integration control signals generated by the integration controller comprise pixel-specific charge accumulation reset signals.

5. (Original): The imager system of claim 4 further comprising an array of memory cells, each memory cell corresponding to a specified pixel in the pixel array and connected to store from the integration controller an indication of number of reset occurrences of the specified pixel during a given imager integration period.

6. (Original): The imager system of claim 5 wherein the memory cell array is configured spatially separate from the pixel array.

7. (Currently Amended): The imager system of claim 5 wherein the output interface circuit comprises ~~a~~ an image data formatter configured to generate output image data based on sense node electrical signals from the pixel array and corresponding reset occurrence data from the memory cell array.

8. (Original): The imager system of claim 5 wherein the integration controller comprises a comparator circuit corresponding to each column of the pixel array, each comparator circuit connected to compare a sense node electrical signal of a pixel selected from the corresponding array

column with a reference electrical signal that is generated based on the dynamic range specification input to produce a comparator output signal determinative of reset timing of the selected pixel.

9. (Original): The imager system of claim 8 wherein the integration controller is configured to generate integration control signals for a selected pixel based on output signals from a corresponding comparator, to permit integration of the selected pixel during at least one of a plurality of integration slots, the integration slots being of successively shorter durations and all integration slots having a common end time, the integration slot durations defined for a given imager integration period based on the dynamic range specification input.

10. (Original): The imager system of claim 9 wherein the plurality of integration slots for a given imager integration period is at least three.

11. (Original): The imager system of claim 1 wherein the output interface circuit comprises a correlated double-sampling circuit configured to convert sense node electrical signals from the pixel array from single-ended to differential output and remove pixel reset level from the sense node electrical signals.

12. (Original): The imager system of claim 11 wherein the output interface circuit further comprises an analog-to-digital converter configured to digitize sense node electrical signals from the pixel array.

13. (Original): The imager system of claim 12 wherein the analog-to-digital converter comprises an array of analog-to-digital converters; and further comprising a multiplexer connected between the pixel array and the

analog-to-digital converter array for directing a selected sense node electrical signal from the pixel array to a selected converter in the array of converters.

14. (Original): The imager system of claim 1 wherein the input interface circuit is further connected to accept a specification of a sub-array of pixels to be controlled in the pixel array; and wherein the integration control circuitry is connected to independently access a selected pixel in the sub-array of pixels.

15. (Original): The imager system of claim 1 wherein the input interface circuit is further connected to accept a specification of a number of pixels to be controlled in the pixel array, and wherein the integration control circuitry is connected to independently access a selected pixel in the number of pixels specified.

16. (Currently Amended): The imager system of claim 1 wherein the input interface circuit is further connected to accept a specification of a frame rate at which images of a scene are to be produced, and wherein the integration control circuitry is configured to impose on the pixel array an imager integration period based on the frame rate specification.

17. (Original): The imager of claim 1 wherein the input interface circuit is further connected to accept a specification of sense node electrical signal digitization resolution, and wherein the output interface circuit comprises an image data formatter configured to generate digitized output image data based on sense node electrical signals and the digitization resolution specification.

18. (Original): The imager system of claim 9 wherein the dynamic range specification input accepted by the input interface circuit comprises a specification of a duration ratio between successively started integration slots for a given imager integration period.

19. (Original): A method for controlling charge integration of a plurality of photosensitive, charge integrating pixels of a pixel array for capturing illumination of a scene to be imaged during an integration period, each pixel comprising a photogenerated charge accumulation region and a sense node at which an electrical signal, indicative of pixel charge accumulation, can be measured without discharging the accumulation region, the method comprising:

(A)providing a plurality of integration slots for the integration period, all integration slots ending with integration period end, a first integration slot beginning with integration period start, and each integration slot following the first slot being of successively shorter duration;

(B)initiating charge integration of each pixel in the pixel array for the integration period and the first integration slot;

(C)for any current integration slot except a last integration slot, at an intermediate time during the current integration slot, evaluating the sense node electrical signal of each pixel for which the current integration slot was initiated to determine if that pixel will saturate during the current integration slot, the saturation evaluation based on the electrical signal range characteristic of that pixel and the ratio of duration of a next succeeding integration slot to duration of the current integration slot;

(D)resetting any pixel for which the integration evaluation indicates pixel saturation during the current integration slot;

(E)permitting continued integration to the end of the current integration slot of any pixel for which the integration evaluation does not

indicate saturation during the current integration slot, and initiating a next succeeding integration slot for any reset pixel;

(F)repeating steps (C) to (E) until the end of the integration period and the last integration slot is reached; and

(G) producing output image data for each pixel based on sense node electrical signals from that pixel and an indication of number of integration slots for which that pixel was initiated during the integration period.

20. (Original): The method of claim 19 wherein the pixel saturation evaluation comprises a comparison of pixel sense node voltage to a check voltage, $V_{CHECK(i)}$, for the i^{th} integration slot, given as:

$$V_{CHECK(i)} = V_{RESET} - \Delta V_D \cdot (1 - \frac{T_{INT(i+1)}}{T_{INT(i)}}), \text{ for electron integration and}$$

$$V_{CHECK(i)} = V_{RESET} + \Delta V_D \cdot (1 - \frac{T_{INT(i+1)}}{T_{INT(i)}}), \text{ for hole integration,}$$

where V_{RESET} is a characteristic pixel reset voltage, ΔV_D is a voltage range characteristic of the pixel, $T_{INT(i+1)}$ is the duration of the next succeeding integration slot, and $T_{INT(i)}$ is the duration of the current integration slot.

21. (Original): The method of claim 19 further comprising updating data stored in an array of memory cells that are provided in a one-to-one correspondence with the array of pixels, memory cell data reflecting a number of times for which a corresponding pixel was reset during the integration period; and wherein the indication of number of integration slots for which a pixel was initiated during the integration period comprises corresponding memory cell data.

22. (Original): The method of claim 19 wherein the plurality of integration slots provided for the integration period comprises at least three integration slots.

23. (Currently Amended): The method of claim 19 wherein the plurality of integration slots provided for the integration period comprise a first integration slot of maximum duration, $T_{INT,MAX}$, and a last integration slot of minimum duration, $T_{INT,MIN}$, which are determined based on an input dynamic range increase specification, K, ~~,~~as $K = \frac{T_{INT,MAX}}{T_{INT,MIN}}$.